presently pending in the subject application and are believed to be allowable over the prior art for at least the reasons advanced below.

35 U.S.C. 103 REJECTION

Claims 1 and 3-6 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,527,737 to Jeng and U.S. Patent No. 5,990,558 to Tran.

1. Summary of the Invention

The claimed invention is directed generally to a method for fabricating a semiconductor device including a step of forming on a substrate a first insulating film with a relatively low dielectric constant and low mechanical strength. The first insulating film is formed locally in a region where capacitance between interconnects is desired to be lowered.

2. The Proposed Combination of References Fail to Disclose the Claimed Invention

Applicant respectfully contends that the claimed invention is clearly patentably distinct over the proposed combination of Jeng and Tran. In particular, it is contended that the combined teachings of Jeng and Tran doe not result in the claimed invention. For instance, Jeng discloses a method for selectively forming a low-dielectric constant insulator layer between metal lines. As shown in Figs. 3-7, insulator layer (12) and contact (11) are formed on the surface of semiconductor body (10), and thereafter a metal layer is deposited on the semiconductor body (10) to form interconnect lines (14a-d). Next, a low-dielectric constant layer (20) is deposited on the semiconductor body (10) such that the areas between the interconnect lines (14a-d) are filled. Further, the low-dielectric constant layer (20) is etched back such that the low-dielectric constant

layer (20) only remains between the interconnect lines (14a-c) and the sidewalls of the interconnect lines (14 a-d). A silicon dioxide layer (18) is then formed to cover the interconnect lines (14a-d) and the low-dielectric constant layer (20). Thereafter, contact vias (24) are patterned and etched through the silicon dioxide layer (18) to be formed in contact with the interconnect lines (14a and 14c). Lastly, the contact vias (24) are buried by a metal layer to formed an interconnect structure shown in Fig. 2.

Secondary reference Tran discloses a method for reducing the cracking of low-dielectric constant layers formed an metal features. As shown in Fig. 2, metal features (11A-B) and (14) are formed on a dielectric layer (10). Next, a HSQ layer (12) is formed as a low-dielectric constant insulator layer to fill the gaps (111) between the metal features (11A-B). Thereafter, upon forming a resist mask on the HSQ layer (12), the HSQ layer (12) is removed from an open field (13) by conventional anisotropic etching. At this time, sidewall spacers (20, 21) are formed on the sidewalls of the metal features (11A-B), and a thin layer of HSQ layer (12) is retained on the metal features (14). The resist mask is then removed, and thereafter a silicon oxide layer (23) composed of TEOS is deposited and planarization of the silicon oxide layer (23) is performed by CMP.

In essence, both Jeng arid Tran disclose methods for forming a structure where a low-dielectric constant insulator layer is selectively buried between metal interconnects formed in advance. Hence, in both Jeng and Tran, the metal connects are formed before the low-dielectric constant insulator layer.

On the other hand, the claimed invention requires, as shown in Figs. 1-3, formation of a low dielectric constant insulating film (101) on a substrate (100) such that no metal interconnect is formed. Thereafter, by selective etching using a mask pattern (102) which is formed on the

low dielectric constant insulating film (101), the low dielectric constant insulating film (101) (HSQ film) is patterned. Next, after forming a p-TEOS film (103) (silicon oxide film) on the substrate (100), the p-TEOS film (103) is planarized by polishing to form a thinned p-TEOS film (103) on the patterned low dielectric constant insulating film (101). A selective etching is then performed using a mask pattern (104) which is formed on the thinned p-TEOS film (103) to form interconnect grooves (104a) in the thinned p-TEOS film (103) and the patterned low dielectric constant insulating film (101). Thereafter, buried interconnects (105) are formed in the interconnect grooves to obtain the interconnect structure shown in Fig. 3(b).

In other words, the claimed invention relates to a method of initially forming an interlayer insulating film composed at the patterned low dielectric constant insulating film (101) and the planarized p-TEOS film (103), and then forming the buried interconnects in the interlayer insulating film. Hence, the interlayer insulating film a composed of the low dielectric constant insulating film is formed before the buried metal interconnects. Such a feature is not taught, disclosed or suggested by the combination of Jeng and Tran.

For the foregoing reasons, the method of forming interconnect structures of Jeng and Tran are completely different from that of the claimed invention. Withdrawal of the rejection is respectfully solicited.

3. Secondary Considerations

As a result of the aforementioned combination of method steps, the claimed invention overcomes the disadvantages associated with conventional fabrication methods. For example, conventionally, when the interconnect pitch is reduced as a result of a reduction of semiconductor integrated circuit devices, it becomes difficult to fill the low dielectric insulating

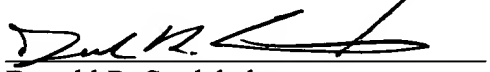
film between interconnects, which disadvantageously restricts the material for the low dielectric insulating film. Also, since the low dielectric insulating film is generally poor in mechanical strength, there arises a problem that defects such as peeling and scratch say be caused in the low dielectric insulating film in planarizing it by the CMP.

In consideration of the aforementioned conventional problems, the present inventors form a low dielectric insulating film between interconnects with a small interconnect pitch and preventing peeling or scratch of the low dielectric insulating film. Thus, in accordance with claim 1 of the present invention, after forming the patterned first insulating film in the first region by patterning the first insulating film with a low dielectric constant and low mechanical strength, the second insulating film with a high dielectric constant and high mechanical strength is formed. Therefore, the first insulating film with a low dielectric constant can be present in the first region alone. Also, since the first insulating film with low mechanical strength is not exposed in planarizing the second insulating film with high mechanical strength by polishing, defects such as peeling and scratch can be prevented from being caused in the first insulating film. Further, since the buried interconnect is formed by filling the metal film in the first interconnect grove formed in the first insulating film with a low dielectric constant, the first insulating film can be definitely disposed between interconnects even when the interconnect pitch is small. Since it has been shown that the proposed combination of Jeng and Tran fails to disclose several steps of the claimed method, the aforementioned non-obvious benefits cannot be achieved.

CONCLUSION

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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